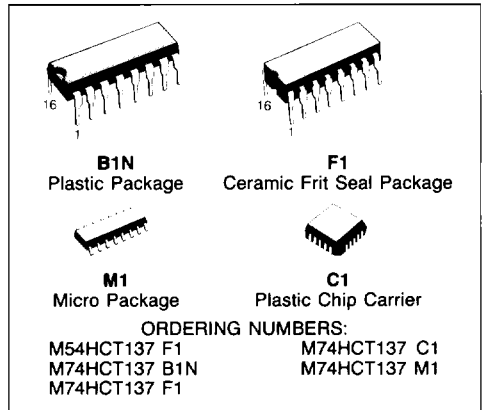


## 3 TO 8 LINE DECODER/LATCH

- **LOW POWER DISSIPATION**  
 $I_{CC} = 4 \mu A$  (MAX.) at  $T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**  
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (MIN.)
- **OUTPUT DRIVE CAPABILITY**  
 10 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**  
 $|I_{OH}| = I_{OL} = 4 \text{ mA}$  (MIN.)
- **BALANCED PROPAGATION DELAYS**  
 $t_{PLH} = t_{PHL}$
- **PIN AND FUNCTION COMPATIBLE**  
 WITH 54/74LS137



### DESCRIPTION

The M54/74HCT137 is a high speed CMOS 3 TO 8 LINE DECODER/LATCH fabricated in silicon gate C<sup>2</sup>MOS technology.

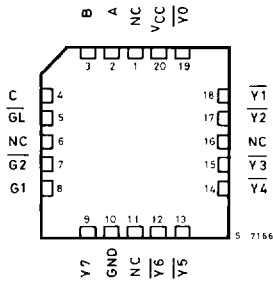
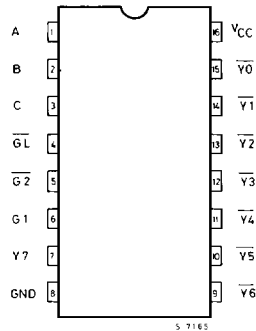
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device is a three-to eight line decoder with latches on the three address inputs. When  $\overline{GL}$  goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as  $\overline{GL}$  remains high no address changes will be recognized. Output enable controls, G1 and G2, control the state of the outputs independently of the select or latch-enable inputs.

All of the outputs are high unless G1 is high and G2 is low. The HCT137 is ideally suited for the implementation of glitch-free decoders in stored address applications in bus oriented systems.

All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuits input and output characteristics are with standard 54/74 LSTTL logic families.

M54HCT/74HCT devices are designed to directly interface HSC<sup>2</sup>MOS systems with TTL and NMOS components. These devices are also plug in replacements for LSTTL devices giving a reduction of power consumption.

### PIN CONNECTIONS (top view)

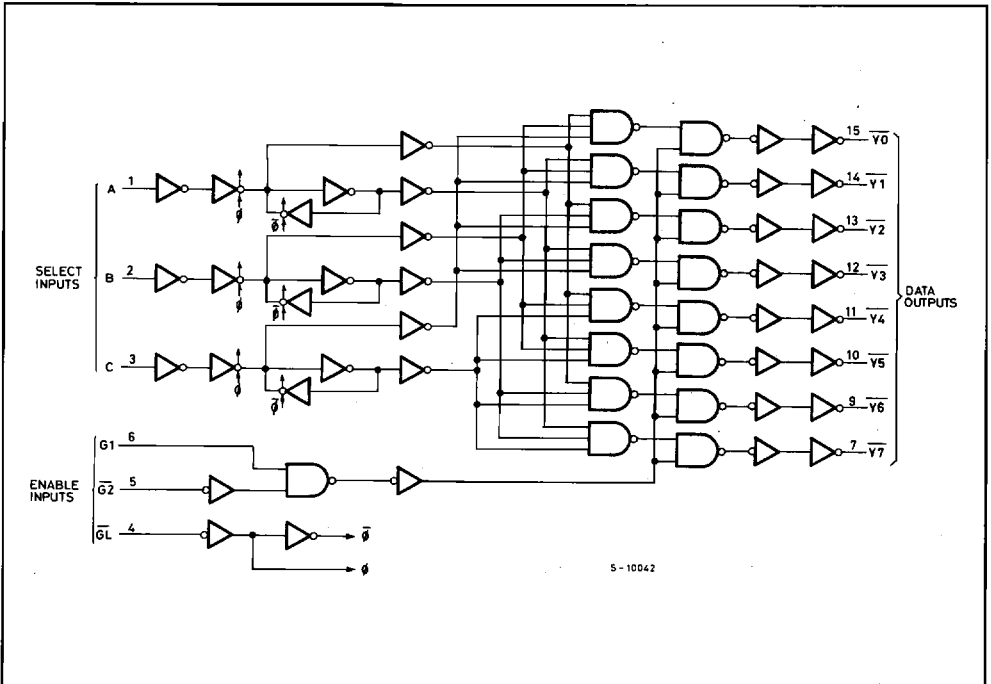


TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT			$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
$\overline{G1}$	$\overline{G2}$	G1	C	B	A								
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	L	L	H	H	L	H	H	H	H
L	L	L	L	H	H	L	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H
L	L	H	H	L	H	H	H	H	L	L	H	H	H
L	L	H	H	H	L	H	H	H	L	L	H	L	H
L	L	H	H	H	H	H	H	H	L	L	H	L	L
H	L	H	X	X	X	OUTPUT CORRESPONDING TO STORED ADDRESS, L; ALL OTHERS, H							

X: DON'T CARE

LOGIC DIAGRAM



5-10042

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to 7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Source Sink Current Per Output Pin	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$P_D$	Power Dissipation	500 (*)	mW
$T_{stg}$	Storage Temperature	-65 to 150	$^{\circ}C$

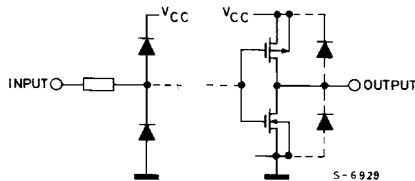
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(\*) 500 mW:  $\cong 65^{\circ}C$  derate to 300 mW by 10 mW/ $^{\circ}C$ :  $65^{\circ}C$  to  $85^{\circ}C$

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	4.5 to 5.5	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_A$	Operating Temperature	74HC Series 54HC Series	- 40 to 85 - 55 to 125	$^{\circ}C$
$t_r, t_f$	Input Rise and Fall Time	0 to 500	ns	

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



## DC SPECIFICATIONS

Symbol	Parameter	V <sub>CC</sub>	Test Condition	T <sub>A</sub> = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit	
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V <sub>IH</sub>	High Level Input Voltage	4.5 to 5.5		2.0	—	—	2.0	—	2.0	—	V	
V <sub>IL</sub>	Low Level Input Voltage	4.5 to 5.5		—	—	0.8	—	0.8	—	0.8	V	
V <sub>OH</sub>	High Level Output Voltage	4.5	V <sub>IN</sub>	I <sub>OH</sub>	4.4	4.5	—	4.4	—	4.4	—	V
			V <sub>IH</sub> or V <sub>IL</sub>	- 20 μA								
				- 4.0 mA								
V <sub>OL</sub>	Low Level Output Voltage	4.5	V <sub>IN</sub>	I <sub>OL</sub>	—	0	0.1	—	0.1	—	0.1	V
			V <sub>IH</sub> or V <sub>IL</sub>	20 μA								
				4.0 mA								
I <sub>IN</sub>	Input Leakage Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND	—	—	±0.1	—	±1	—	±1	μA	
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND	—	—	4	—	40	—	80	μA	
I <sub>CC</sub>			Per input: V <sub>IN</sub> = 0.5V or 2.4V Other input: V <sub>CC</sub> or GND	—	—	2.0	—	2.9	—	3.0	mA	

AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C, C<sub>L</sub> = 15pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time		4	8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (G1-Y)		21	34	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (G2-Y)		20	32	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (GL-Y)		29	46	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (A, B, C-Y)		25	39	ns

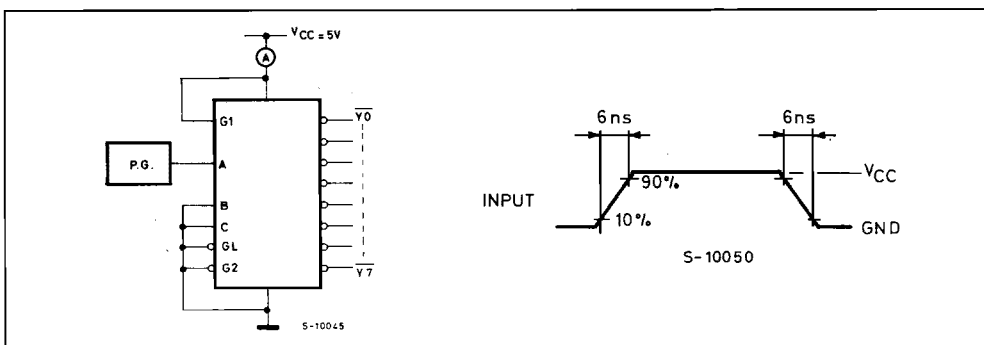
AC ELECTRICAL CHARACTERISTICS ( $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$ )

Symbol	Parameter	$V_{CC}$	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			$-40$ to $85^\circ\text{C}$ 74HC		$-55$ to $125^\circ\text{C}$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
$t_{TLH}$ $t_{THL}$	Output Transition Time	4.5		—	8	15	—	19	—	22	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time ( $G1-\bar{Y}$ )	4.5		—	25	39	—	49	—	59	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time ( $G2-\bar{Y}$ )	4.5		—	24	37	—	46	—	56	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time ( $GL-\bar{Y}$ )	4.5		—	34	52	—	65	—	78	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (A, B, C- $\bar{Y}$ )	4.5		—	29	45	—	56	—	68	ns
$t_{W(L)}$	Minimum Pulse Width ( $\bar{G}L$ )	4.5		—	8	15	—	19	—	22	ns
$t_s$	Minimum Set-up Time (A, B, C- $\bar{G}L$ )	4.5		—	2	10	—	13	—	15	ns
$t_h$	Minimum Hold Time (A, B, C- $\bar{G}L$ )	4.5		—	—	5	—	5	—	5	ns
$C_{IN}$	Input Capacitance			—	5	10	—	10	—	10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	68	—	—	—	—	—	pF

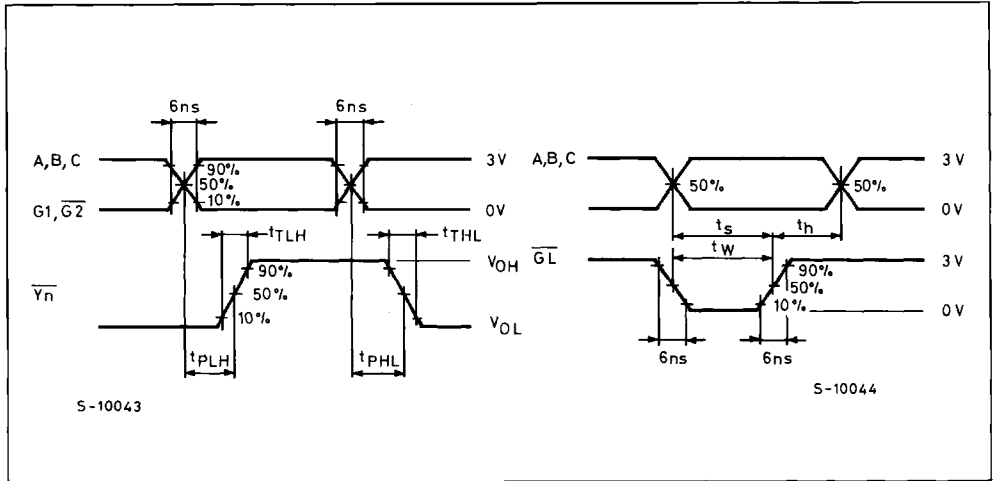
Note (\*)  $C_{PD}$  is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the equation:  $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

## TEST CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM



TYPICAL APPLICATION

